

2N3418(S) - 2N3421(S) Series

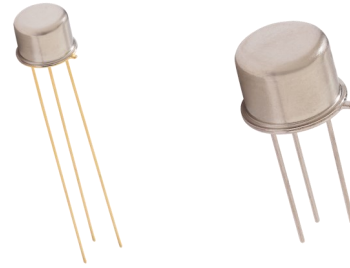


NPN Medium Power Silicon Transistor

Rev. V4

Features

- Available in JAN, JANTX, JANTXV, JANS and JANSR 100K rads(Si) per MIL-PRF-19500/393
- TO-5 & TO-39 (TO-205AD) Packages
- Ideal for Medium Power Applications Requiring High Frequency Switching



Electrical Characteristics ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Parameter | Test Conditions | Symbol | Units | Min. | Max. |
|--|---|---------------|------------------|--|---|
| Off Characteristics | | | | | |
| Collector - Emitter Breakdown Voltage | $I_C = 50 \text{ mA dc}$ 2N3418, S, 2N3420, S 2N3419, S, 2N3421, S | $V_{(BR)CEO}$ | V dc | 60 80 | — |
| Collector - Emitter Cutoff Current | $V_{CE} = 80 \text{ Vdc}, V_{BE} = -0.5 \text{ Vdc}$ 2N3418, S, 2N3420, S $V_{CE} = 120 \text{ Vdc}, V_{BE} = -0.5 \text{ Vdc}$ 2N3419, S, 2N3421, S | I_{CEX1} | $\mu\text{A dc}$ | — | 0.3 0.3 |
| Collector - Emitter Cutoff Current | $V_{CE} = 45$ 2N3418, S, 2N3420, S $V_{CE} = 60$ 2N3419, S, 2N3421, S | I_{CEO} | $\mu\text{A dc}$ | — | 5.0 5.0 |
| Emitter - Base Cutoff Current | $V_{EB} = 6 \text{ Vdc}, I_C = 0$ $V_{EB} = 8 \text{ Vdc}, I_C = 0$ | I_{EBO} | $\mu\text{A dc}$ | — | 0.5 10.0 |
| On Characteristics¹ | | | | | |
| Forward Current Transfer Ratio | $I_C = 100 \text{ mA dc}, V_{CE} = 2 \text{ V dc}$ 2N3418, S, 2N3419, S 2N3420, S, 2N3421, S $I_C = 1 \text{ A dc}, V_{CE} = 2 \text{ V dc}$ 2N3418, S, 2N3419, S 2N3420, S, 2N3421, S $I_C = 2 \text{ A dc}, V_{CE} = 2 \text{ V dc}$ 2N3418, S, 2N3419, S 2N3420, S, 2N3421, S $I_C = 5 \text{ A dc}, V_{CE} = 5 \text{ V dc}$ 2N3418, S, 2N3419, S 2N3420, S, 2N3421, S | H_{FE} | - | 20 40 20 40 15 30 10 15 | — — 60 120 — — — — |
| Base - Emitter Voltage | $I_C = 1 \text{ A dc}, I_B = 0.1 \text{ A dc}$ $I_C = 2 \text{ A dc}, I_B = 0.2 \text{ A dc}$ | $V_{BE(SAT)}$ | Vdc | 0.6 0.7 | 1.2 1.4 |
| Collector - Emitter Saturation Voltage | $I_C = 1 \text{ A dc}, I_B = 0.1 \text{ A dc}$ $I_C = 2 \text{ A dc}, I_B = 0.2 \text{ A dc}$ | $V_{CE(SAT)}$ | Vdc | — | 0.25 0.50 |

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| Parameter | Test Conditions | Symbol | Units | Min. | Max. |
|------------------------------------|---|------------|------------------|------|----------|
| Collector - Emitter Cutoff Current | $T_A = +150^{\circ}\text{C}$ $V_{CE} = 80 \text{ Vdc}, V_{BE} = -0.5 \text{ Vdc}$ 2N3418, S, 2N3420, S $V_{CE} = 120 \text{ Vdc}, V_{BE} = -0.5 \text{ Vdc}$ 2N3419, S, 2N3421, S | I_{CEX2} | $\mu\text{A dc}$ | — | 16 16 |
| Forward Current Transfer Ratio | $T_A = -55^{\circ}\text{C}$ | h_{fe5} | | 10 | |

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Electrical Characteristics ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Parameter | Test Conditions | Symbol | Units | Min. | Max. |
|---|---|------------|---------------|------|------|
| Dynamic Characteristics | | | | | |
| Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio | $I_C = 0.1 \text{ A dc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 20 \text{ MHz}$ | $ h_{fe} $ | - | 1.3 | 8.0 |
| Output Capacitance | $V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$ | C_{obo} | pF | — | 150 |
| Switching Characteristics | | | | | |
| Delay Time | $V_{BE(off)} = -3.7 \text{ Vdc}$; $I_C = 1 \text{ A dc}$; $I_{B2} = 100 \text{ mA dc}$ | t_d | μs | — | 0.08 |
| Rise Time | | t_r | | | 0.22 |
| Storage Time | $V_{BE(off)} = -3.7 \text{ Vdc}$; $I_C = 1 \text{ A dc}$; $I_{B2} = 100 \text{ mA dc}$ | t_s | μs | — | 1.10 |
| Fall Time | | t_f | | | 0.20 |
| Safe Operating Area | | | | | |
| DC Tests: | $T_C = +100^\circ\text{C}$, 1 Cycle, $t = 1.0 \text{ s}$ | | | | |
| Test 1: | $V_{CE} = 5 \text{ Vdc}$, $I_C = 3.0 \text{ A dc}$ | | | | |
| Test 2: | $V_{CE} = 37 \text{ Vdc}$, $I_C = 0.4 \text{ A dc}$ | | | | |
| Test 3: | $V_{CE} = 60 \text{ Vdc}$, $I_C = 0.185 \text{ mA dc}$ 2N3418, S; 2N3420, S | | | | |
| | $V_{CE} = 80 \text{ Vdc}$, $I_C = 0.120 \text{ mA dc}$ 2N3419, S; 2N3421, S | | | | |

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Ratings | Symbol | Value 2N3418, S 2N3420, S | Value 2N3419, S 2N3421, S |
|--|------------------------------|---------------------------------|---------------------------------|
| Collector - Emitter Voltage | V_{CEO} | 60 Vdc | 80 Vdc |
| Collector - Base Voltage | V_{CBO} | 85 Vdc | 125 Vdc |
| Emitter - Base Voltage | V_{EBO} | 8 Vdc | |
| Collector Current $T_P \leq 1 \text{ ms}$, duty cycle $\leq 50\%$ | I_C | 3 Adc 5 Adc | |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$ ¹ @ $T_C = 100^\circ\text{C}$ ¹ | P_T | 1 W 5 W | |
| Operating & Storage Temperature Range | T_J , T_{STG} | -65°C to +200°C | |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ ³ | 175 °C/W | |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ ³ | 18 °C/W | |

- (1) For derating, see figures 4, 5 and 6 of MIL-PRF-19500/393
 (2) This value applies for $t_p \leq 1 \text{ ms}$, duty cycle ≤ 50 percent
 (3) For thermal impedance curves see figures 7, 8 and 9 of MIL-PRF-19500/393

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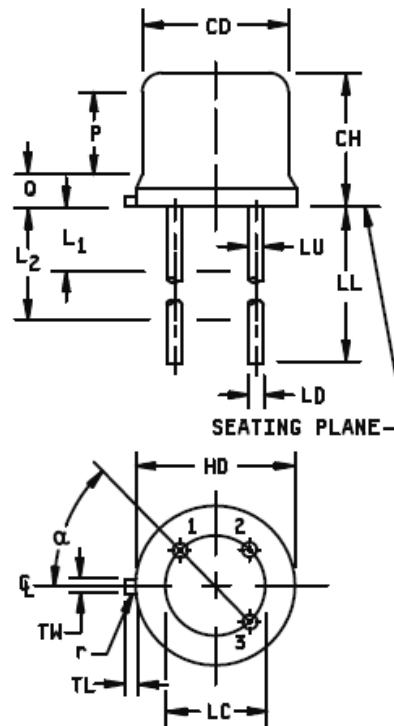


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Outline Drawing (TO-5 & TO-39)

| Symbol | Dimensions | | | | Note |
|----------------|---------------------|------|-------------|-------|------|
| | Inches | | Millimeters | | |
| | Min | Max | Min | Max | |
| CD | .305 | .335 | 7.75 | 8.51 | |
| CH | .240 | .260 | 6.10 | 6.60 | |
| HD | .335 | .370 | 8.51 | 9.40 | |
| LC | .200 TP | | 5.08 TP | | 6 |
| LD | .016 | .021 | 0.41 | 0.53 | |
| LL | .500 | .750 | 12.7 | 19.05 | 7 |
| LU | See notes 7, 13, 14 | | | | |
| L ₁ | | .050 | | 1.27 | 7 |
| L ₂ | .250 | | 6.35 | | 7 |
| P | .100 | | 2.54 | | 5 |
| Q | | .040 | | 1.02 | 4 |
| TL | .029 | .045 | 0.74 | 1.14 | 3,10 |
| TW | .028 | .034 | 0.71 | .86 | 9,10 |
| r | | .010 | | 0.25 | 11 |
| α | 45° TP | | 45° TP | | 6 |



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. Lead number 3 is electrically connected to case.
9. Beyond r maximum, TW shall be held for a minimum length of .021 inch (0.53 mm).
10. Lead number 4 omitted on this variation.
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N3418S, 2N3419S, 2N3420S, 2N3421S, LL is .500 (12.70 mm) minimum and .750 (19.05 mm) maximum (short leads).
13. For transistor types 2N3418, 2N3419, 2N3420, 2N3421, LL is 1.500 (38.10 mm) minimum, and 1.750 (44.45 mm) maximum (long leads).
14. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
15. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.

FIGURE 1. Physical dimensions.

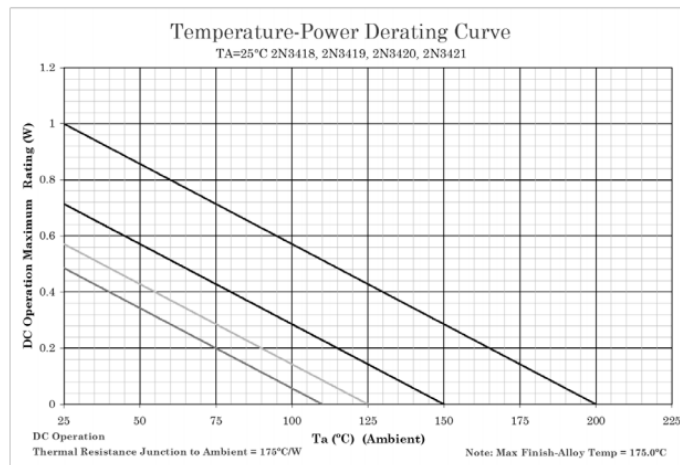
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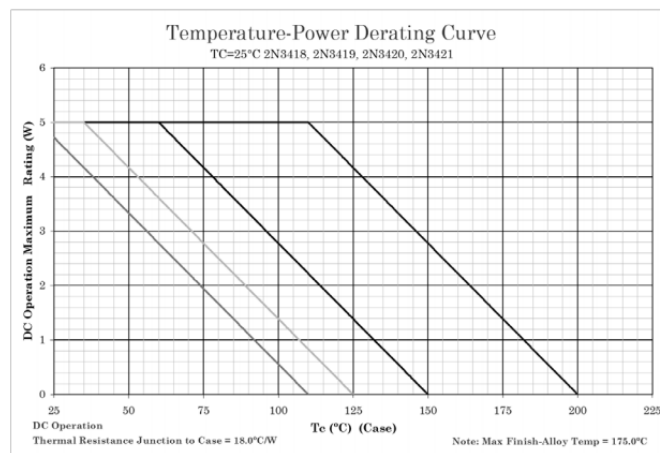
Temperature-Power Derating Curves



NOTES:

1. All devices are capable of operating at T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 4. Derating for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S ($R_{\theta JA}$) leads .375 inch (9.53 mm) PCB (TO-5 and TO-39).



NOTES:

1. All devices are capable of operating at T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Derating for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S ($R_{\theta JC}$) (TO-5 and TO-39).

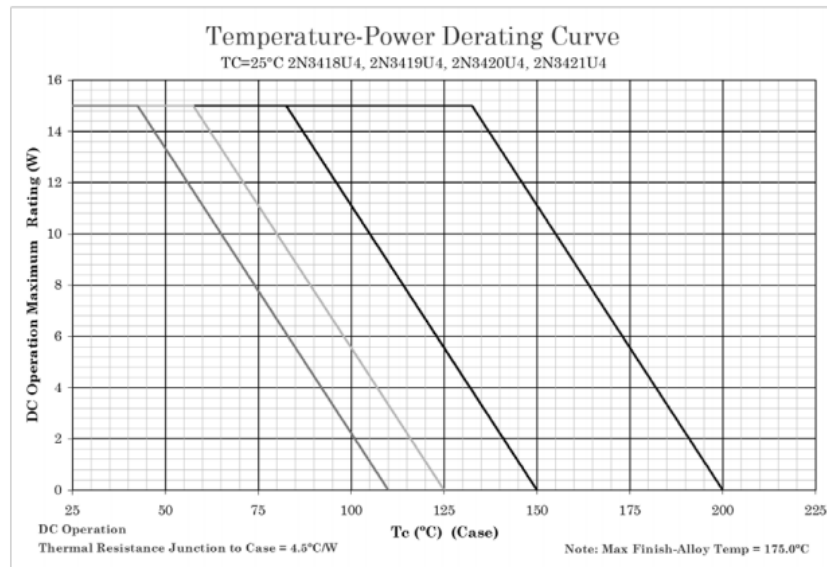
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Temperature-Power Derating Curves



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Derating for 2N3418U4, 2N3419U4, 2N3420U4, and 2N3421U4 ($R_{\theta JC}$) (U4).

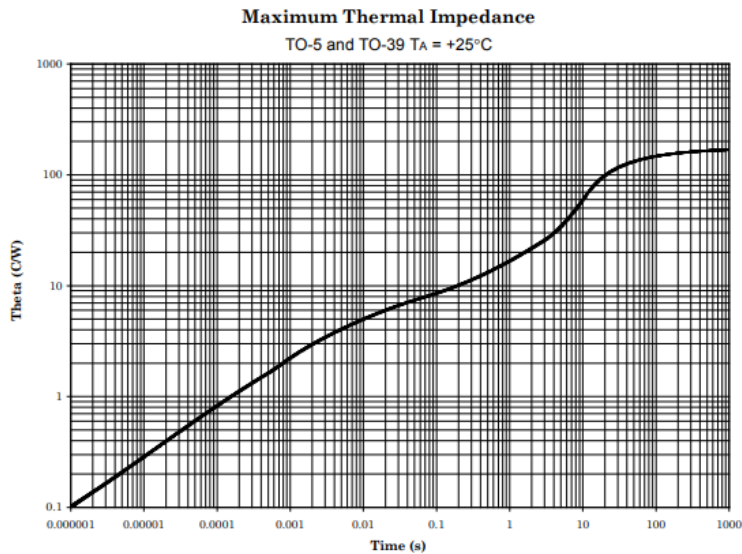
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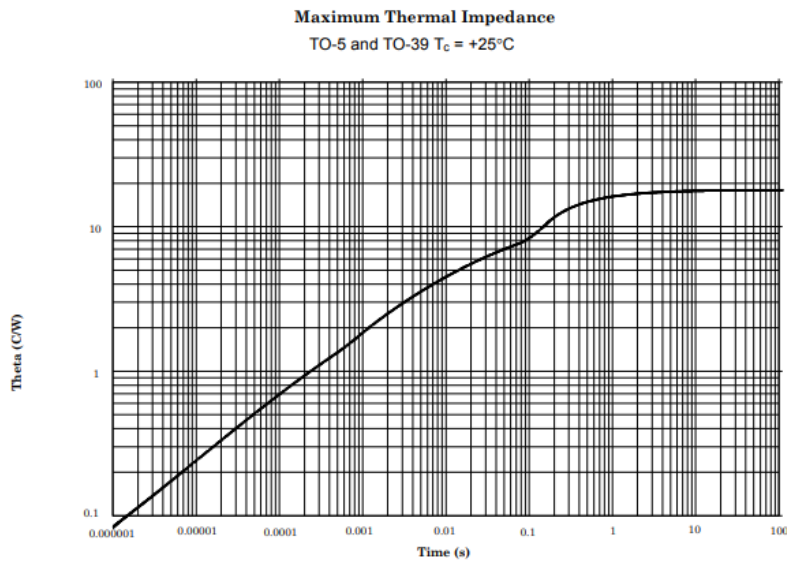
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Thermal Impedance Curves



$T_A = +25^\circ\text{C}$, $P_{\text{diss}} = 1.0 \text{ W}$, Thermal Resistance $R_{\theta JA} = 175^\circ\text{C/W}$

FIGURE 7. Thermal impedance graph ($R_{\theta JA}$) for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S leads .375 inch PCB (TO-5 and TO-39).



$T_C = +25^\circ\text{C}$, Thermal Resistance $R_{\theta JC} = 18^\circ\text{C/W}$

FIGURE 8. Thermal impedance graph ($R_{\theta JC}$) for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S (TO-5 and TO-39).

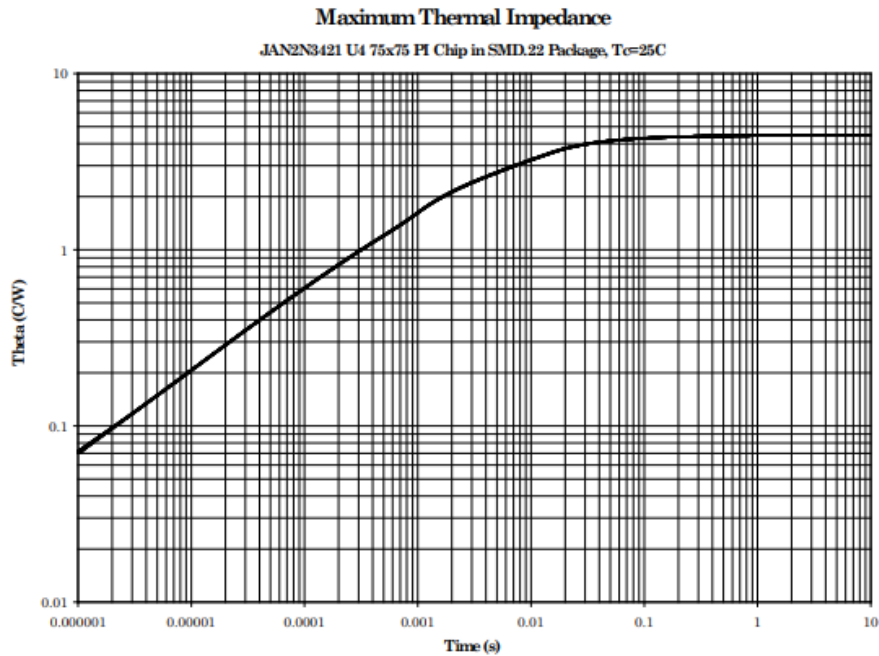
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Thermal Impedance Curves



T_c = +25°C, Thermal Resistance R_{θJC} = 4.5°C/W, R_{θJX} = 3.25°C/W at 10ms

FIGURE 9. Thermal impedance graph (R_{θJC}) for 2N3418U4, 2N3419U4, 2N3420U4 and 2N3421U4 PCB (U4).

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