

# 2N1711, 2N1711S 2N1890, 2N1890S

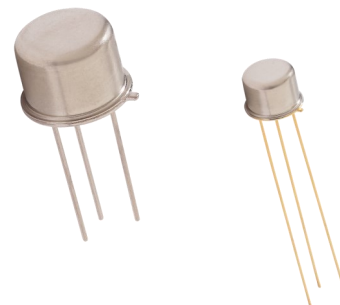


## NPN Low Power Silicon Transistor

Rev. V1

### Features

- Available in JAN, JANTX and JANTXV per MIL-PRF-19500/225
- TO-5 and TO-39 Packages
- General Purpose Transistors for Low Power Applications
- Ideal for High Performance Low Noise Amplifiers, Oscillators and Switching Circuits



### Electrical Characteristics (25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	$I_C = 30 \text{ mA dc}$ 2N1711, 2N1711S 2N1890, 2N1890S	$V_{(BR)CEO}$	V dc	30 60	—
Collector - Emitter Breakdown Voltage	$I_C = 100 \text{ mA dc}$ , $R_{BE} = 10 \Omega$ 2N1711, 2N1711S 2N1890, 2N1890S	$V_{(BR)CER}$	V dc	50 80	—
Collector - Base Cutoff Current	$V_{CB} = 60 \text{ V dc}$ 2N1711, 2N1711S $V_{CB} = 80 \text{ V dc}$ 2N1890, 2N1890S	$I_{CBO1}$	nA dc	—	10 10
Emitter - Base Cutoff Current	$V_{EB} = 5 \text{ Vdc}$	$I_{EBO1}$	nA dc	—	5.0
Collector - Base Cutoff Current	$V_{CB} = 75 \text{ V dc}$ 2N1711, 2N1711S $V_{CB} = 100 \text{ V dc}$ 2N1890, 2N1890S	$I_{CBO2}$	$\mu\text{A dc}$	—	100 100
Emitter - Base Cutoff Current	$V_{EB} = 7 \text{ Vdc}$	$I_{EBO2}$	$\mu\text{A dc}$	—	100
Collector-Emitter Saturation Voltage	$I_C = 150 \text{ mA dc}$ , $I_B = 15 \text{ mA dc}$ 2N1711, 2N1711S 2N1890, 2N1890S	$V_{CE(SAT)1}$	V dc	—	1.5 5.0
Collector-Emitter Saturation Voltage	$I_C = 50 \text{ mA dc}$ , $I_B = 5 \text{ mA dc}$ , 2N1890, 2N1890S	$V_{CE(SAT)2}$	V dc	—	1.2
Base-Emitter Saturation Voltage	$I_C = 150 \text{ mA dc}$ , $I_B = 15 \text{ mA dc}$ 2N1711, 2N1711S 2N1890, 2N1890S	$V_{BE(SAT)1}$	V dc	—	1.3 1.3
Base-Emitter Saturation Voltage	$I_C = 50 \text{ mA dc}$ , $I_B = 5 \text{ mA dc}$ 2N1890, 2N1890S	$V_{BE(SAT)2}$	V dc	—	0.9

# 2N1711, 2N1711S 2N1890, 2N1890S



## NPN Low Power Silicon Transistor

Rev. V1

### Electrical Characteristics (25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Forward - Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}; I_C = 10 \mu\text{A dc}$ $V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc}$	$h_{FE1}$ $h_{FE2}$		20 100	300
Forward - Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc}$ 2N1711, 2N1711S	$h_{FE3}$		50	
Collector Base Cutoff Current	$T_A = 150^\circ\text{C}$ $V_{CB} = 60 \text{ V dc}, 2\text{N}1711, 2\text{N}1711\text{S}$ $V_{CB} = 80 \text{ V dc}, 2\text{N}1890, 2\text{N}1890\text{S}$	$I_{CB03}$	$\mu\text{A dc}$	—	10 15
Forward - Current Transfer Ratio	$T_A = -55^\circ\text{C}$ $V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc}$	$h_{FE4}$		35	
Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ mA dc}; f = 1 \text{ kHz}$ $V_{CE} = 10 \text{ V dc}; I_C = 5 \text{ mA dc}; f = 1 \text{ kHz}$	$h_{fe1}$ $h_{fe2}$		80 90	200 270
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}; I_C = 50 \text{ mA dc}; f = 20 \text{ MHz}$	$ h_{fe} $		3.5	12
Small-Signal Short-Circuit Input Impedance	$V_{CB} = 10 \text{ V dc}; I_C = 5 \text{ mA dc}; f = 1 \text{ kHz}$	$h_{ib}$	$\Omega$	4	8
Small-Signal Short-Circuit Input Admittance	$V_{CB} = 10 \text{ V dc}; I_C = 5 \text{ mA dc}; f = 1 \text{ kHz}$ 2N1711, 2N1711S 2N1890, 2N1890S	$h_{ob}$	$\mu\text{mhos}$	0.0 0.0	1.0 .3
Small-Signal Open-Circuit Reverse Voltage Transfer Ratio	$V_{CB} = 10 \text{ V dc}; I_C = 5 \text{ mA dc}; f = 1 \text{ kHz}$ 2N1711, 2N1711S 2N1890, 2N1890S	$h_{rb}$	$\mu\text{mhos}$		$5 \times 10^{-4}$ $1.5 \times 10^{-4}$
Open Circuit Output Capacitance	$V_{CB} = 10 \text{ V dc}; I_E = 0 \text{ mA dc};$ $f = 100 \text{ kHz} \leq f \leq 1 \text{ MHz}$ 2N1711, 2N1711S 2N1890, 2N1890S	$C_{obo}$	pF	8 5	25 15
Pulse Response	Test condition A, except test circuit and pulse requirements. See figure 6 of MIL-PRF-19500/225	$t_{on} + t_{off}$	ns		30

# 2N1711, 2N1711S 2N1890, 2N1890S



## NPN Low Power Silicon Transistor

Rev. V1

### Absolute Maximum Ratings (25°C unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage 2N1711, 2N1711S 2N1890, 2N1890S	$V_{CEO}$	30 V dc 60 V dc
Collector - Emitter Voltage 2N1711, 2N1711S 2N1890, 2N1890S	$V_{CER}$	50 V dc 80 V dc
Collector - Base Voltage 2N1711, 2N1711S 2N1890, 2N1890S	$V_{CBO}$	75 V dc 100 V dc
Emitter - Base Voltage	$V_{EBO}$	7 V dc
Collector Current	$I_C$	500 mA dc
Total Power Dissipation @ $T_C = +25^\circ\text{C}$ @ $T_A = +25^\circ\text{C}$	$P_T^{(2)}$	3.0 W 0.8 W
Junction & Storage Temperature Range	$T_J, T_{STG}$	-65°C to +200°C

### Thermal Characteristics <sup>(3)</sup>

Characteristics	Symbol	Max. Value
Thermal Resistance Junction to Case	$R_{\theta JC}$	30°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	175°C/W

- (1) Also applies to the corresponding "S" suffix device.  
 (2) For derating see figure 2 and figure 3 as shown on pages 5 and 6.  
 (3) For thermal impedance curves see figure 4 and figure 5 on pages 7 and 8.

# 2N1711, 2N1711S 2N1890, 2N1890S

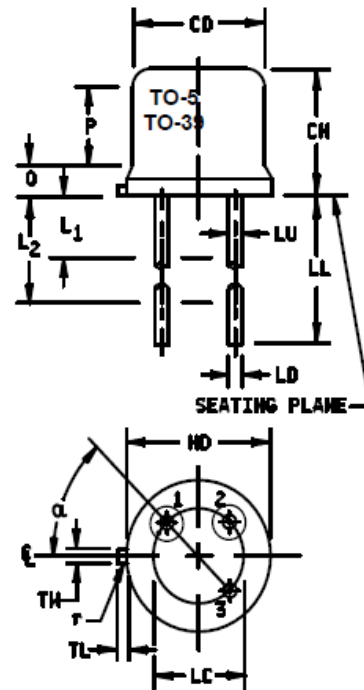


NPN Low Power Silicon Transistor

Rev. V1

## Outline Drawing: TO-5, TO-39 Package Types

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TYP		5.08 TYP		7
LD	.016	.021	0.41	0.53	6
LL	See notes 7, 9, and 10				
LU	.016	.019	0.41	0.48	7
L <sub>1</sub>		.050		1.27	7
L <sub>2</sub>	.250		6.35		7
P	.100		2.54		5
Q		.050		1.27	
r		.010		0.254	8
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	3
α	45° TP		45° TP		6
Term 1	Emitter				
Term 2	Base				
Term 3	Collector				



### NOTES:

- Dimensions are in inches.
- Millimeters are given for general information only.
- Beyond r maximum, TW must be held to a minimum length of .021 inch (0.53 mm).
- TL measured from maximum HD.
- CD shall not vary more than  $\pm 0.010$  inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
- Leads at gauge plane .054 - .055 inch (1.37 - 1.40 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at a maximum material condition (MMC) relative to the tab at MMC. The device may be measured by direct methods or by gauge and gauging procedure.
- LU applies between L<sub>1</sub> and L<sub>2</sub>. LD applies between L<sub>2</sub> and L minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
- r (radius) applies to both inside corners of tab.
- \* 9. For transistor types 2N1711S and 2N1890S, LL is .500 inch (12.70 mm) minimum, and .750 inch (19.05 mm) maximum (TO-39).
10. For transistor types 2N1711 and 2N1890, LL is 1.500 inches (38.10 mm) minimum, and 1.750 inches (44.45 mm) maximum (TO-5).
11. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

\* FIGURE 1. Physical dimensions (TO-5 and TO-39).

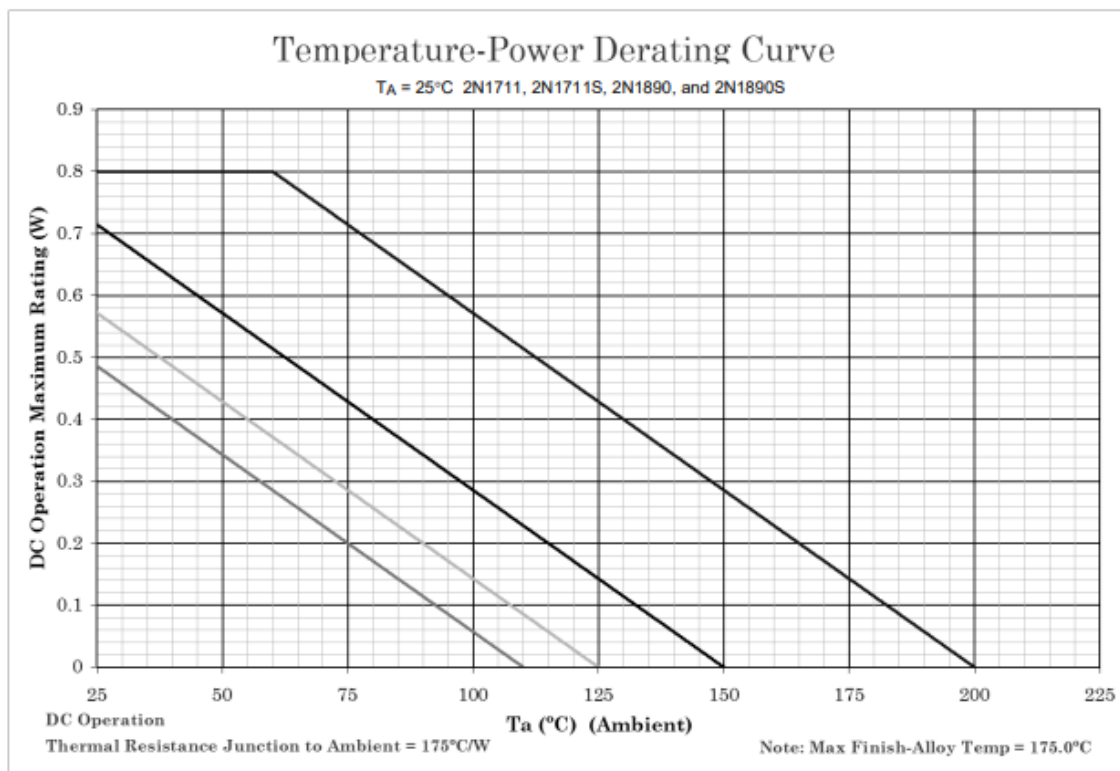
# 2N1711, 2N1711S 2N1890, 2N1890S



NPN Low Power Silicon Transistor

Rev. V1

## Temperature-Power Derating Curve



### NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 2. Temperature-power derating for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).

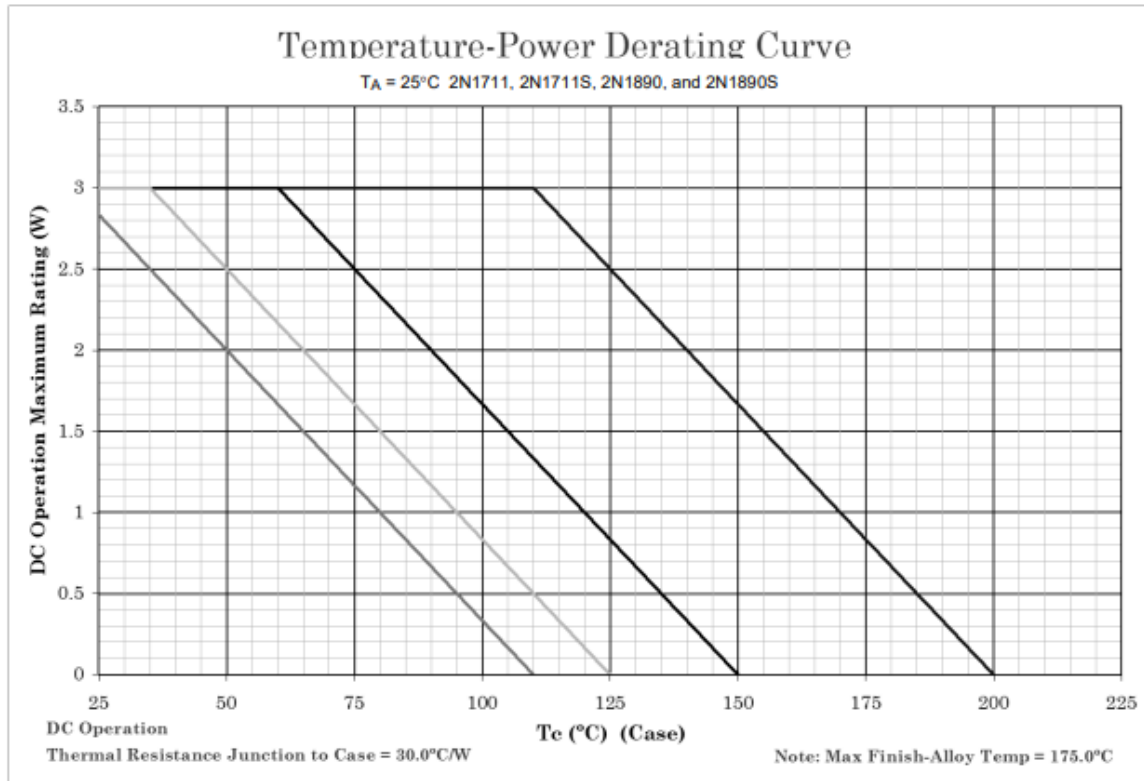
# 2N1711, 2N1711S 2N1890, 2N1890S



NPN Low Power Silicon Transistor

Rev. V1

## Temperature-Power Derating Curve



### NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 3. Temperature-power derating for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).

# 2N1711, 2N1711S 2N1890, 2N1890S



NPN Low Power Silicon Transistor

Rev. V1

## Thermal Impedance Curves

### Maximum Thermal Impedance

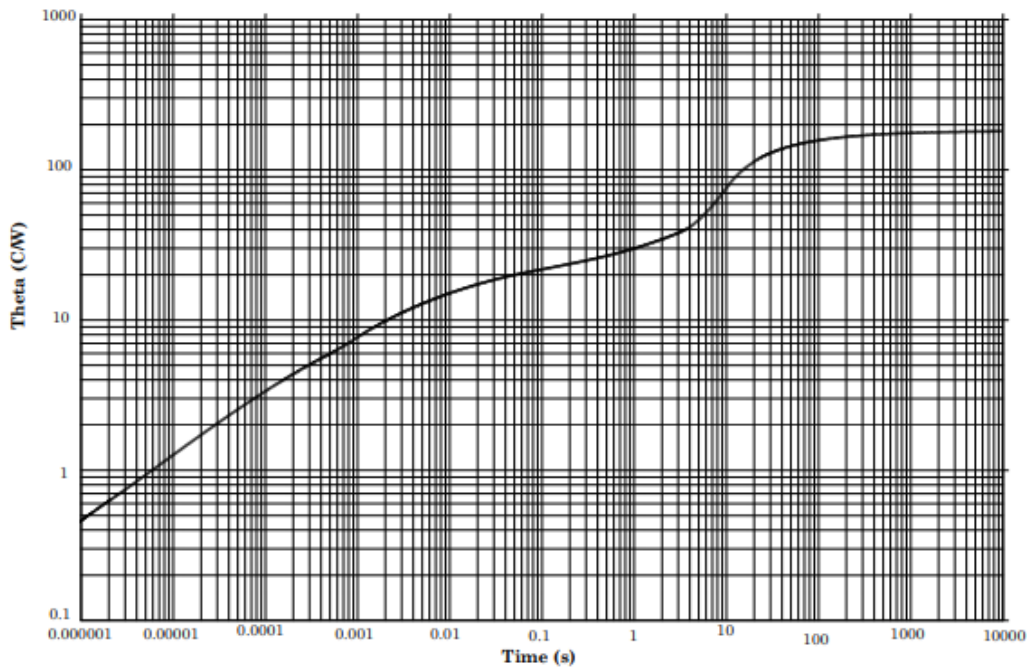


FIGURE 4. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).

# 2N1711, 2N1711S 2N1890, 2N1890S



NPN Low Power Silicon Transistor

Rev. V1

## Thermal Impedance Curves

### Maximum Thermal Impedance

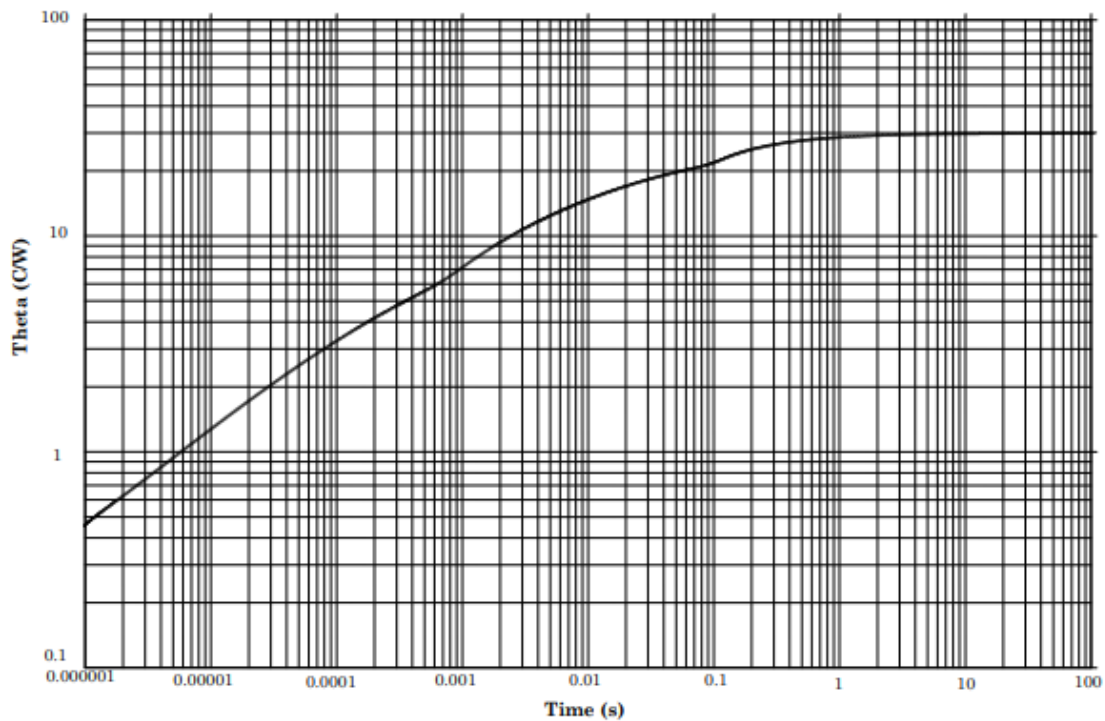


FIGURE 5. Thermal impedance graph ( $R_{\theta JC}$ ) for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).



# 2N1711, 2N1711S 2N1890, 2N1890S



NPN Low Power Silicon Transistor

Rev. V1

## VPT COMPONENTS. ALL RIGHTS RESERVED.

Information in this document is provided in connection with VPT Components products. These materials are provided by VPT Components as a service to its customers and may be used for informational purposes only. Except as provided in VPT Components Terms and Conditions of Sale for such products or in any separate agreement related to this document, VPT Components assumes no liability whatsoever. VPT Components assumes no responsibility for errors or omissions in these materials. VPT Components may make changes to specifications and product descriptions at any time, without notice. VPT Components makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF VPT COMPONENTS PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. VPT COMPONENTS FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. VPT COMPONENTS SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

VPT Components products are not intended for use in medical, lifesaving or life sustaining applications. VPT Components customers using or selling VPT Components products for use in such applications do so at their own risk and agree to fully indemnify VPT Components for any damages resulting from such improper use or sale.