

## NPN General Purpose Silicon Transistor Amplifier Die

Rev. V1

### Features

- JEDEC Registered 2N3904
- Designed For Low Noise Amplifier Applications
- High Gain, Low Saturation Voltage



### Electrical Characteristics ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
<b>Off Characteristics</b>					
Collector - Emitter Breakdown Voltage	$I_C = 1.0 \text{ mA dc}, I_B = 0$	$V_{(BR)CEO}$	V dc	40	—
Collector - Base Breakdown Voltage	$I_C = 10 \mu\text{A dc}, I_E = 0$	$V_{(BR)CBO}$	V dc	60	—
Emitter - Base Breakdown Voltage	$I_E = 10 \mu\text{A dc}, I_C = 0$	$V_{(BR)EBO}$	V dc	6.0	—
Base Cutoff Current	$V_{CE} = 30 \text{ V dc}, V_{EB} = 3 \text{ V dc}$	$I_{BL}$	nA dc	—	50
Collector Cutoff Current	$V_{CE} = 30 \text{ V dc}, V_{EB} = 3 \text{ V dc}$	$I_{CEX}$	nA dc	—	50
<b>On Characteristics</b>					
Forward Current Transfer Ratio	$V_{CE} = 1.0 \text{ V dc}, I_C = 0.1 \text{ mA dc}$ $V_{CE} = 1.0 \text{ V dc}, I_C = 1.0 \text{ mA dc}$ $V_{CE} = 1.0 \text{ V dc}, I_C = 10 \text{ mA dc}$ $V_{CE} = 1.0 \text{ V dc}, I_C = 50 \text{ mA dc}$ $V_{CE} = 1.0 \text{ V dc}, I_C = 100 \text{ mA dc}$	$h_{FE}$	-	40 70 100 60 30	300
Collector - Emitter Saturation Voltage	$I_C = 10 \text{ mA dc}, I_B = 1.0 \text{ mA dc}$ $I_C = 50 \text{ mA dc}, I_B = 5.0 \text{ mA dc}$	$V_{CE(sat)}$	V dc	—	0.2 0.3
Base - Emitter Saturation Voltage	$I_C = 10 \text{ mA dc}, I_B = 1.0 \text{ mA dc}$ $I_C = 50 \text{ mA dc}, I_B = 5.0 \text{ mA dc}$	$V_{BE(sat)}$	Vdc	0.65	0.85 0.95
<b>Small Signal Characteristics</b>					
Current Gain - Bandwidth Product	$V_{CE} = 20 \text{ V dc}, I_C = 10 \text{ mA dc}$ $f = 100 \text{ MHz}$	$f_T$	MHz	300	
Output Capacitance	$V_{CB} = 5.0 \text{ V dc}, I_E = 0, f = 100 \text{ kHz}$	$C_{obo}$	pF		4.0
Input Capacitance	$V_{EB} = 0.5 \text{ V dc}, I_C = 0, f = 100 \text{ kHz}$	$C_{ibo}$	pF		8.0
Noise Figure	$V_{CE} = 5.0 \text{ V dc}, I_C = 100 \mu\text{A dc}$ $R_S = 1.0 \text{ k}\Omega,$ $f = 10 \text{ Hz to } 15.7 \text{ kHz}$	NF	dB		5.0

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Switching Characteristics					
Parameter	Test Conditions	Symbol	Units	Min.	Max.
Delay Time	$V_{CC} = 3.0 \text{ V dc}$ , $V_{BE} = 0.5 \text{ V dc}$ $I_C = 10 \text{ mA}$ , $I_{B1} = 1.0 \text{ mA}$	$t_d$	ns	—	35
Rise Time	$V_{CC} = 3.0 \text{ V dc}$ , $V_{BE} = 0.5 \text{ V dc}$ $I_C = 10 \text{ mA}$ , $I_{B1} = 1.0 \text{ mA}$	$t_r$	ns	—	35
Storage Time	$V_{CC} = 3.0 \text{ V dc}$ , $I_C = 10 \text{ mA dc}$ $I_{B1} = I_{B2} = 1.0 \text{ mA dc}$	$t_s$	ns		200
Fall Time	$V_{CC} = 3.0 \text{ V dc}$ , $I_C = 10 \text{ mA dc}$ $I_{B1} = I_{B2} = 1.0 \text{ mA dc}$	$t_f$	ns	—	50

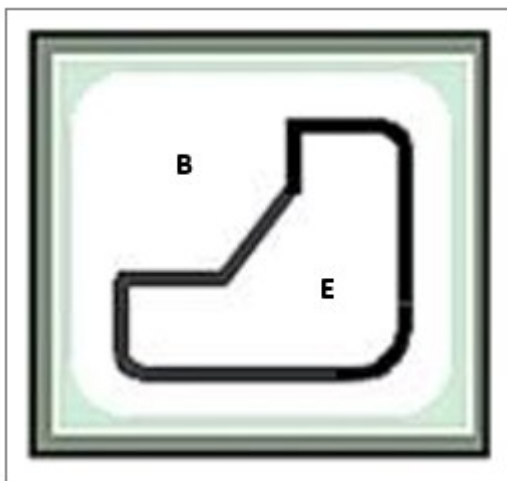
Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	$V_{CEO}$	40 V dc
Collector - Base Voltage	$V_{CBO}$	60 V dc
Emitter - Base Voltage	$V_{EBO}$	6.0 V dc
Collector Current	$I_C$	200 mA dc
Operating & Storage Temperature Range	$T_J$ , $T_{STG}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$

## Notes:

1. These ratings are based on maximum junction temperature of  $150^\circ\text{C}$
2. These are steady-state limits. VPT Components should be consulted on applications involving pulsed or low-duty cycle

## Outline Drawing (Chip)



Length	Width	Bond Pads	Thickness
0.010	0.010	0.003 x 0.003 (+0.0005)	0.007

**Notes:**

1. All dimensions are in inches.
2. All tolerances are  $\pm 0.002$  inches unless otherwise noted.
3. Top Side Metallization: Aluminum (20kÅ)
4. Back Side Metallization: Gold (8kÅ)
5. **B** = Base, **E** = Emitter, **C** = Collector (Backside of the die).

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